AMENDMENTS TO THE SPECIFICATION

In the Title of the Invention:

Please **CHANGE** the title to read:

SHIFT REGISTER ADOPTING A DATA CONVERSION CONTROL SYSTEM AND DRIVING CIRCUIT OF A LCD USING THE SAME

In the Specification:

Please **AMEND** the specification as shown in the following marked up paragraph, which shows changes made relative to the immediate prior version.

Please **AMEND** the paragraph beginning on **page 8, line 6** as follows:

The above-described configuration of a shift register employing delay units, illustrated and explained with reference to FIGs. 2 and 3, can be also applied to a m row x n column matrix configuration. Specifically, the column of D flip flops M0, M1, M2, M3, shown in FIG. 2 correspond, respectively, to the column of D flip flops M00, M01, M02, M03, shown in FIG. 4. Though not shown in FIG. 4, delay units similar to the delay units 32, 34, 36 shown in FIG. 2 may be connected to the D flip flops M00, M01, M02, M03, respectively, in a manner similar to that illustrated in, and described in reference to, FIGs. 2 and 3.

Please **AMEND** the paragraph beginning on **page 8, line 11** as follows:

The first column of the matrix consists of D flip flops M00, M01, M02, M03, the second column of the matrix consists of D flip flops M04, M05, M06, M07, the third column of the

matrix consists of D flip flops M08, M09, M10, M11, and the fourth column of the matrix consists of D flip flops M12, M13, M14, M15.

Please **AMEND** the paragraph beginning on **page 8, line 15** as follows:

D flip flops M00, M04, M08, M12 constituting the first row have input terminals with switching logics 40, 42, 44, 46, respectively. Each of [[S]]switching logics 40, 42, 44, 46 classifies input data D00, D10, D20, D30 into positive and negative, and selectively outputs the data to the corresponding D flip flop by a first switching control signal.

Please **AMEND** the paragraph beginning on **page 8, line 19** as follows:

D flip flops M03, M07, M11, M15 constituting the fourth row have output terminals with switching logics 50, 52, 54, 56, respectively. Each of [[S]]switching logics 50, 52, 54, 56 classifies data output from D flip flops M03, M07, M11, M15 into positive and negative, and selectively outputs data D01, D11, D21, D31 by a second switching control signal.

Please **AMEND** the paragraph beginning at **page 9, line 6** as follows:

To shift the flag signal, D flip flops MF0, MF1, MF2, MF3 are configured ~~of~~ the ~~counts~~ same as those ~~of~~ in each row of the matrix, and constitute a ~~row~~ ~~column~~. D flip flops MF0, MF1, MF2, MF3 are shift comparing ~~shift~~ registers. The flag signal is shifted passing through D flip flops MF0, MF1, MF2, MF3, and is inputted as the second switching control signal of switching logics 50, 52, 54, 56.

Please **AMEND** the paragraph beginning at **page 10, line 5** as follows:

Under the assumption that data "0000" is stored in D flip flops M00, M04, M08, M12 of the first row, respectively, and that data to be input D00, D10, D20, D30 is "1111", the D flip flops M00, M04, M08, M12 of the first row shift[[,]] when clock signal CLK is input[[,]] to transfer the stored data "0000" to D flip flops M01, M05, M09, M13 of the second row and to receive and store the new data "1111". However, in this case, all of D flip flops M00, M04, M08, M12 ~~of~~ in the first row ~~shift~~ require current supply for converting from logic "0" to logic "1". If D flip flops constituting the matrix perform the above-described data conversion all at once ~~in their entirety~~, a significant amount of instantaneous power supply is needed.

Please **AMEND** the paragraph beginning at **page 10, line 13** as follows:

In the first embodiment of the present invention, data D02, D12, D22, D32, which are divided from the data to be input to the first row, and data D03, D13, D23, D33, output from D flip flops constituting the first row, are compared in the shift comparing unit 60[[.]] ~~This~~ to prevent[[s]] data conversion that may require a huge volume of power supply.

Please **AMEND** the paragraph beginning at **page 12, line 4** as follows:

Each of [[S]]switching logics 40, 42, 44, 46 inverts the state of input data and outputs the result to D flip flops M00, M04, M08, M12[[,]] when the first switching control signal is fed from the shift comparing unit 60 as logic "1". Then, the flag signal for recognizing conversion of data for the corresponding row is input to D flip flop MF0, which constitutes ~~constituting~~ the

shift comparing register. The flag signal to be stored in D flip flop MF1 is synchronized with clock CLK and shifted like other data stored in D flip flops D00, D04, D08, D12 of the first row.

Please **AMEND** the paragraph beginning at **page 12, line 11** as follows:

When data state change is estimated in three or more D flip flops of each row, the data being input is converted and stored in the corresponding D flip flop, and the corresponding flag is stored. In this manner, data conversion of flip flops can be maintained at a minimum, while at the same time reducing instantaneous power supply, and preventing the occurrence of EMI.

Please **AMEND** the paragraph beginning at **page 12, line 16** as follows:

When thus-stored data and flag are shifted, D flip flops M03, M07, M11, M15 of the last row output data, and the flag signal is output from the last D flip flop of the shift comparing ~~shift~~ register.

Please **AMEND** the paragraph beginning at **page 12, line 21** as follows:

Therefore, each of switching logics 50, 52, 54, 56 invert data output from D flip flops M03, M07, M11, M15 constituting the last row of the shift register and output data D01, D11, D21, D31 when the flag signal, i.e.., the second switching control signal, is applied as logic "1".

Please **AMEND** the paragraph beginning at **page 13, line 2** as follows:

When data is stored as "0000" in D flip flops M02, M04, M08, M12 of the first row and data D00, D10, D20, D30 are input as "1111", switching logics 40, 42, 44, 46 invert the state of

data D00, D10, D20, D30 and input "0000" to D flip flops M00, M04, M08, M12. Here, the flag signal generated together with the first switching control signal applied to switching logics 40, 42, 44, 46, is stored in D flip flop MF0 of the shift comparing ~~shift~~ register.

Please **AMEND** the paragraph beginning at **page 13, line 8** as follows:

When such data and flag signal are synchronized with the clock signal[[,]] and the gradually shifted[[,]] output from D flip flops M03, M07, M11, M15 of the last-row, and input to switching logics 50, 52, 54, 56, data of logic "0000" is inverted into the original state "1111" by the second switching control signal output from D flip flop MF3 of the shift comparing register.